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EXAMINER	
RAHMAN, FAHMIDA	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,397	UEDA, TADAYOSHI	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 are pending.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 1 19(a)-(d). The certified copy filed on 11/5/2003 has been received.

Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 1 19(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

Specification

The disclosure is objected to because of the following informalities:

"fist" in line 5 of [0008] and line 2 of [0009] of page 4 should be changed to "first".

Appropriate correction is required.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "S5" has been used to designate both "VDET setting change" and "REG recovery" in Fig 5, and "S6" has been used to designate both "VDET Recovery" and "REG Setting Change" in Fig 5.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 2 is objected to because of the following informalities: "fist" in line 14 in claim 2 should be changed to "first".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 2 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not

described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 2 recites the limitation "changing the second switching signal from a first to second condition; wherein said control section changes the second switching signal from the first to second condition after changing the first switching signal from the first to second condition when the power saving mode is set, wherein said control section returns the second switching signal to the second condition after returning the first switching signal to the first condition when the power saving mode is terminated".

The enablement of claim 2 is disclosed in Fig 4 and Fig 5, pages 11-13 in applicant's specification.

Claim 2 requires changing of the second switching signal from the first to second condition **after** changing the first switching signal from the first to second condition when the power saving mode is set.

However, the specification describes that the second switching signal is changed from the first to second condition **before** changing the first switching signal from the first to second condition when the power saving mode is set ([0034] of page 12 of applicant's specification mentions that VDET switching signal (or the second switching signal) is

changed from 130 down to 50 values and then, the REG setting signal (or the first switching signal) is changed from 127 down to 48 values).

Additionally, claim 2 requires control section return the second switching signal to the **second** condition after returning the first switching signal to the first condition when the power saving mode is terminated.

However, page 13 of [0035] of applicant's specification mention that the REG setting signal (or first switching signal) is returned from 48 to 127 values and then changes VDET setting signal (or second switching signal) from 50 to 130 values. Thus, the specification enables control section to return the second switching signal to the **first** condition after returning the first switching signal to the first condition when the power saving mode is terminated.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitation "a first to second condition" in line 9. It is unclear whether it is intended to be the same or different from "a first to second condition" recited in line 5.

It is necessary to establish a relationship between the two recitations of "a first to second condition".

The ambiguities and lack of enablement in claim 2 preclude a reasonable search of the prior art by Examiner. Accordingly, claim 2 has not been treated on the merits.

Claim 3 depends on claim 2. Thus, they carry the same ambiguity of claim 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admission of prior art, in view of Saitou (US Patent 5696979).

Applicant admits that the following limitations exist in prior art:

A power supply system (VBAT and 5 in Fig 6) **for supplying power to a CPU** (2 in Fig 6), **said power supply system comprising:**

- **a power supply circuit for supplying the CPU with a prescribed supply voltage** (Fig 6 shows that the prescribed voltage is 2V);

- **a voltage detecting circuit for outputting a reset signal for resetting the CPU when the supply voltage is at or below a prescribed voltage detection value** (lines 4-7 in [0005] of page 3 in applicant's specification mention that the voltage detecting circuit outputs reset when supply is below reference);

- **a control circuit for decreasing the supply voltage to a prescribed power save voltage level when a power saving mode is set, wherein the control circuit decreases the supply voltage to be the prescribed power save voltage level** (lines 7-9 of [0005] of page 3; lines 7-8 of [0004] of page 3 in applicant's specification mention that regulator is signaled to decrease the output from regulator under a power saving mode and the voltage detecting section detects such a decreased voltage in the power saving mode. Thus, the circuit decreases the supply voltage to a power save voltage level when a power saving mode is set)

Applicant's admission of prior art does not teach the following limitations:

decreasing the voltage **after decreasing the prescribed voltage detection value to be less than or equal to the power save voltage level when the power saving**

mode is set, and wherein said control circuit recovers the prescribed voltage detection value after recovering the supply voltage when the power saving mode is terminated.

Saitou teaches the following limitations:

A control circuit (circuit of Fig 2) **decreases the supply voltage** (lines 54-57 of column 1 and lines 1-5 of column 2 mention that the microcomputer enters a stand-by mode when a voltage of the main power line drops and the detected voltage from the voltage detection circuit is below a prescribed stand-by set voltage. Thus, the control circuit of Fig 2 decreases the supply voltage of main power line 1 below stand-by set voltage. In stand-by mode, microcomputer stops power supply to components except for RAM and other backup sections. Thus, the control circuit decreases the supply voltage to the components of microcomputer in stand-by mode of the microcomputer) **after decreasing the voltage detection value** ("detected voltage" in Fig 2) **to be less than the power save voltage level** ("stand-by set voltage" in lines 56-57 of column 1) **when the power saving mode is set** (lines 54-57 of column 1 and lines 1-5 of column 2 mention that the microcomputer enters a stand-by mode when a voltage of the main power line drops and the detected voltage from the voltage detection circuit is below a prescribed stand-by set voltage. The control circuit of Fig 2 decreases the supply voltage of main power line 1 below stand-by set voltage. In stand-by mode, microcomputer stops power supply to components except for RAM and other backup

sections. Thus, turning off the switch 51 can be thought as the setting of power saving mode), **and wherein said control circuit recovers the voltage detection value after recovering the supply voltage when the power saving mode is terminated** (lines 65-67 of column 2 mention that the power source is on/off by external manipulation. Lines 3-5 of column 3 mention that the voltage detecting circuit detects voltage of main power line and outputs a detected voltage indicative of voltage of said main power line. Thus, when the power save mode is terminated by turning the switch 51 on, the circuit recovers the detected voltage after recovering the supply voltage**).**

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teachings of applicant's admission of prior art and Saitou. One ordinary skill in the art would have been motivated to have the circuit for decreasing the detection value to be less than power save voltage when the power saving mode is set and recovers the voltage detection level when the power save mode is terminated, as taught by Saitou, since that would ensure the correct entry of the processor into the power save mode. The processor has to know a voltage detection value to switch to the proper power state.

However, the combination of applicant's admission of prior art and Saitou does not teach the decrease and recovery of the prescribed detection voltage.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmae (US Patent 5237698), in view of Saitou (US Patent 5696979).

For claim 4, Ohmae teaches the following limitations:

A method for supplying power to a CPU (Fig 1 and Fig 2) providing a power saving mode ("standby mode" as described in lines 58-63 of column 1), said method comprising the steps of:

- **providing a reset signal for resetting the CPU when an output voltage from a power supply is less than or equal to a prescribed operable level** (lines 36-39 and lines 42-46 of column 3 mention that the reset circuit 5 supplies reset signal 12 when voltage is 2V or lower);
- **setting a power saving mode** ("standby mode" in lines 10-15 of column 3);
- decreasing the prescribed operable level (the prescribed voltage 2V is blocked or decreased by 6 and 7 to produce "0" volt when standby mode is set. Lines 60-61 of column 3 mention clearly that such steps cause the initial reset operating voltage to be lower);
- **resetting the power saving mode** ("operating mode" of CPU causes resetting "standby mode");
- **and recovering the prescribed operable level after recovering the output voltage** (6 and 7 do not block the prescribed voltage. Thus, 2V operable level is

recovered to reset CPU after the CPU is set at normal operating voltage. In other words, the prescribed operable level 2V is recovered to reset CPU in normal operating mode when the output voltage for normal operation is recovered)

Ohmae does not teach the following limitations:

Decreasing the level of voltage before decreasing the output voltage down to power save voltage.

Saitou teaches decreasing of the operable level (the "detected voltage" in Fig 2 is decreased when SW51 is turned off) before decreasing the output voltage to power save mode (microcomputer is set at standby mode after detected voltage is less than threshold at A/D terminal as mentioned in lines 54-57 of column 1).

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teachings of Saitou and Ohmae. One ordinary skill in the art would have been motivated to decrease the operable level of Ohmae before decreasing the output voltage down to power save mode as taught by Saitou, since that would ensure the correct operation of CPU and reset. For example, the initial reset circuit of Ohmae may output reset signal at 3V, instead of 2V. In such a case, CPU enters standby mode after SB signal is set to "1", while 6, 7 and 4 block the prescribed operable level to output the reset signal from AND gate as soon as SB signal is set. Thus, the prescribed

operable level is decreased before the power save mode is set when initial reset circuit is set at 3V to produce reset signal.

Allowable Subject Matter

Claim 3 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116